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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARC BEAUJOIN, THOMAS ALOFS,
and PAUL ARMAGNAT

Appeal 2008-003253[1]
Application 10/075,113
Technology Center 2100

Decided:[2] July 2, 2009

Before JOHN C. MARTIN, JAY P. LUCAS, and
ST. JOHN COURTENAY III, *Administrative Patent Judges.*

MARTIN, *Administrative Patent Judge.*

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[1] The real party in interest is STMicroelectronics SA.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) (2002) from the Examiner's final rejection of claims 9, 11, 12, 14-17, 20-23, and 26-29.[3] Claims 10, 13, 18, 19, 24, 25, 30, and 31 stand objected to for depending on rejected claims.[4]

We have jurisdiction under 35 U.S.C. § 6(b) (2002). We affirm.

A. Appellants' invention

Appellants' invention concerns testing of sequential access memories, in particular first in/first out (FIFO) memories, using a dedicated test circuit integrated during fabrication of the memory and an associated test algorithm. Specification 1:2-6.

Appellants' Figure 1 is reproduced below.

[3] Final Action dated March 7, 2006 ("Final Action") at 5, 8.
[4] Final Action at 5.

FIG.1

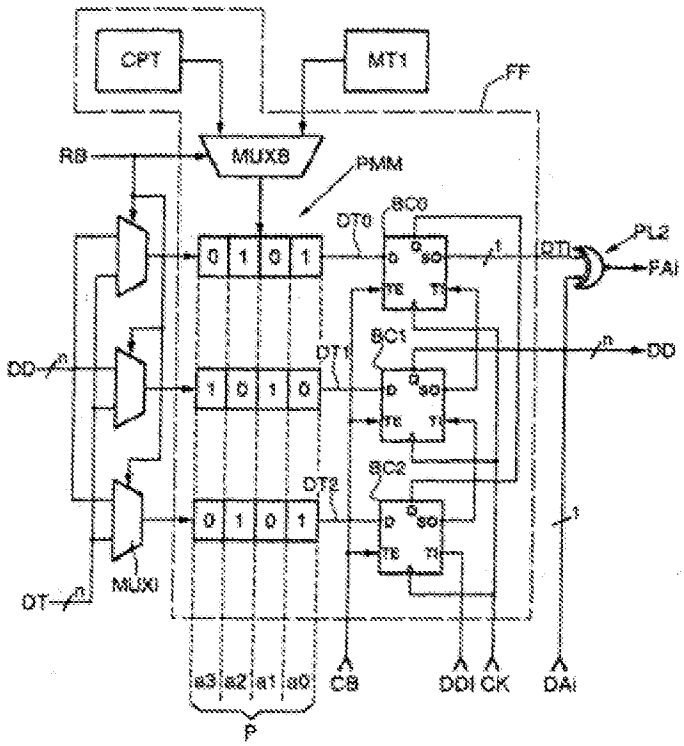

Figure 1 is a diagram showing one embodiment of a memory device according to the invention. *Id.* at 5:7-8. Sequential access memory device FF includes a memory array PMM that can store p words (e.g., a0, a1, a2, a3) having n bits (with p=4 and n=3 in Fig. 1). *Id.* at 5:12-18. During the normal mode of operation, data bits DD on the bus are written into the memory array via multiplexers MUXi. *Id.* at 5:31-33. In the test mode of operation, test data bits DT are written into the memory array via those multiplexers. *Id.* at 5:33-35.

Memory device FF further includes n output registers BC0-BC2, which are shown as D-type flip-flops each having a data input D connected to a respective one of the n outputs of the memory plane PMM. *Id.* at

6:12-15. Each flip-flop D, which is clocked by a clock signal CK, also has a data output Q, a test input TI, a test output SO, and a test control input TE. *Id.* at 6:15-19.

In the normal mode of operation, the n data bits extracted from the memory PMM are delivered to the respective n data inputs D of the flip-flops and are then transferred to the n data outputs Q in time with the rising edges of clock signal CK. *Id.* at 6:20-24.

The test mode of operation employs the fact that the flip-flops are chained together by connecting the test output SO of one flip-flop (e.g., flip-flop BC1) to the test input TI of the adjacent flip-flop (e.g., flip-flop BC0). *Id.* at 6:27-33. When the control signal CB applied to test control inputs TE takes the value 0, the data bit at the input D of a flip-flop is delivered to its own test output SO on the next rising edge of the clock CK. *Id.* at 7:5-10. Then, when the signal CB takes the value 1, each flip-flop delivers the data bit at its test input TI (i.e., the data bit from test output SO of the adjacent flip flop) to its own output SO in time with the rising edges of the clock signal CK. *Id.* at 7:10-15.

Figure 2 is reproduced below.

FIG.2

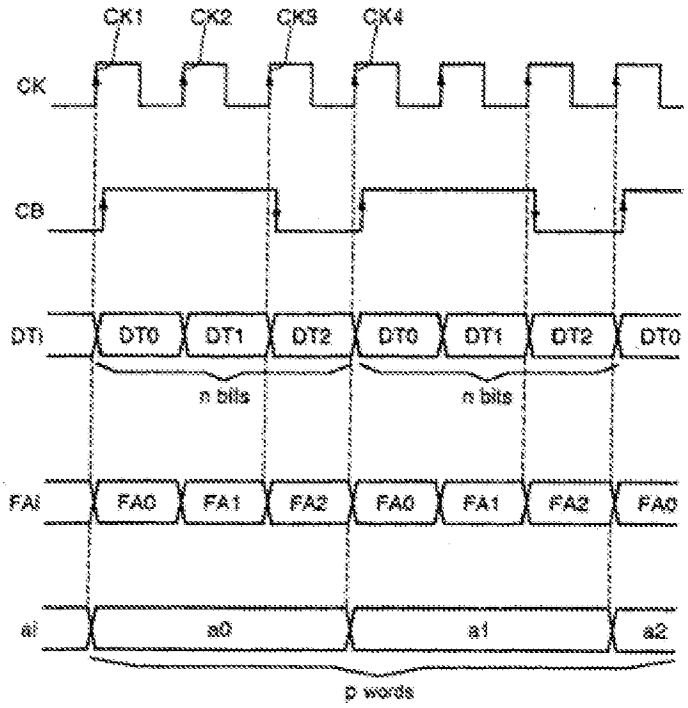

Figure 2 is a timing diagram illustrating one embodiment of the method according to the invention. *Id.* at 5:9-10. This figure shows that the test words (a0, a1, a2, a3) are extracted in sequence from the memory and that the test bits (DT0, DT1, DT2) of each word are applied in sequence to logic gate PL2, which compares each test bit to the expected data bit DAi, the results of the comparison being indicated by the values FA0-FA2 in the logic gate output signal FAi. *Id.* at 8:20 to 9:36.

B. The claims

The independent claims before us are claims 9, 11, 14, 20, and 26, of which claim 11 reads:

> 11. A method of testing a sequential access memory array, the method comprising:
>
> writing test words each made up of a plurality of

> test bits in the memory array;
>
> sequentially extracting the test words from the memory array; and
>
> comparing the test bits of the extracted test words with expected data bits so that for each test word extracted, the corresponding test bits are compared sequentially with respective expected data bits before extracting the next test word.

Claim App., Br. 14.

C. The references and rejections

The Examiner relies on the following references:

Martens	US 5,751,727	May 12, 1998
Kim et al. (Kim)	US 6,108,802	Aug. 22, 2000
Zorian et al. (Zorian)	US 6,330,696 B1	Dec. 11, 2001

Claims 9, 11, 14-17, 20-23, and 26-29 stand rejected under 35 U.S.C. § 103(a) for obviousness over Kim in view of Martens.

Claim 12 stands rejected under § 103(a) for obviousness over Kim in view of Martens and Zorian.

Appellants argue the merits of all of the rejected claims as a single group. Br. 7. We select claim 11 as a representative claim. 37 C.F.R. § 41.37(a)(1)(vii) (2008)[5]; *In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987).

THE ISSUES

Generally speaking, the issue is whether Appellants have shown reversible error by the Examiner in maintaining the rejection. *See In re*

[5] This provision was also in effect when the Brief was filed.

Kahn, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (Citation omitted).

The principal issue before us is whether Appellants have shown that the Examiner erred in finding that Martens discloses (1) sequentially extracting the test words from the memory array and (2) sequentially comparing the test bits of the extracted test words with the expected data bits for each extracted test word. Another issue is whether it would have been obvious in view of Kim to apply Martens's teachings to a sequential access memory.

PRINCIPLES OF LAW

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). On appeal to the Board, appellants "can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness." *Kahn*, 441 F.3d at 985-86.

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). "[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 417.

WHETHER MARTENS DISCLOSES SEQUENTIAL WORD EXTRACTION AND SEQUENTIAL BIT COMPARISON

Although the Examiner based the rejection on Kim in view of Martens, we begin our analysis with Martens.

Martens discloses dynamic latch circuits for use in high-speed array designs (Martens, col. 1, ll. 11-14), such as SRAMs (static random access memories). *Id.* at col. 2, ll. 46-52.

Figure 3 of Martens is reproduced below.

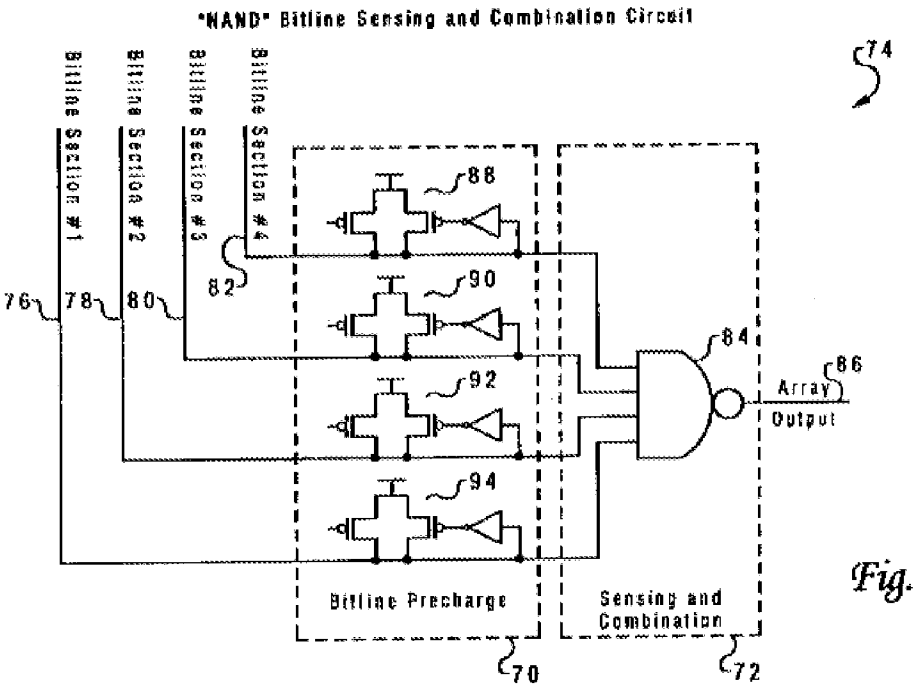

Fig. 3

Figure 3 depicts a NAND bitline sensing and combination circuit 74 used to implement Marten's invention. *Id.* at col. 4, ll. 51-53. The bitline is provided in sections, as shown in Figure 1b (not reproduced herein), in order to reduce the capacitance seen by the array cell that will be discharging the bitline. *Id.* at 4, ll. 18-22. The sensing and combination circuit 74 of Figure 3 includes a bitline precharge section 70 and a NAND-implemented sensing and combination section 72, the latter section including NAND gate

logic 84 that provides the array output 86 for the bitline. *Id.* at col. 4, ll. 53-56.

Figure 4 is reproduced below.

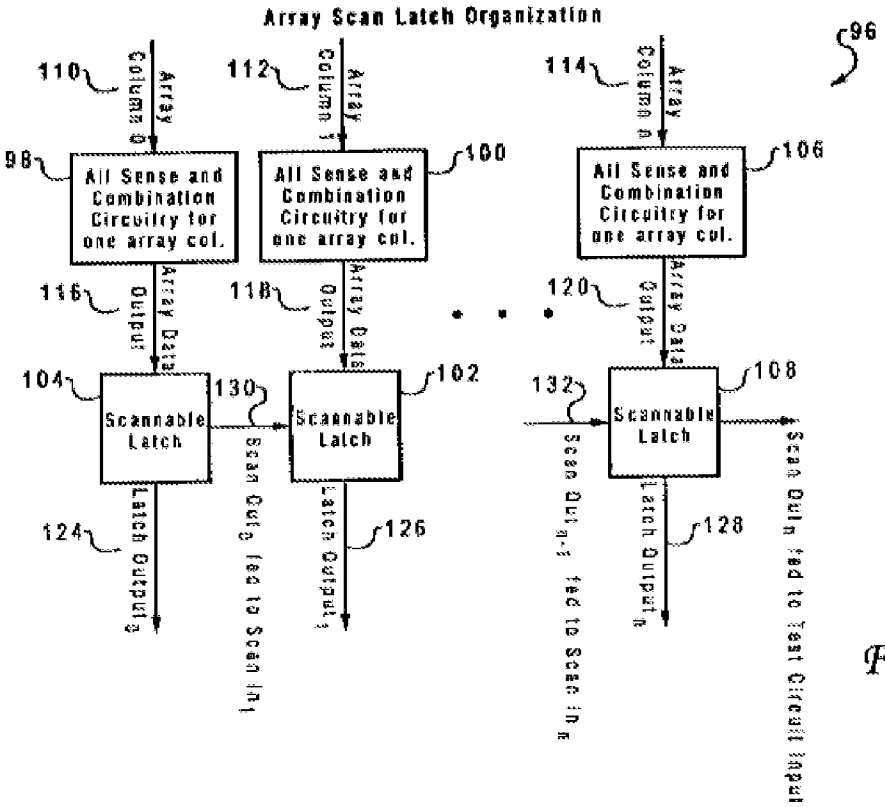

Fig. 4

Figure 4 illustrates a block diagram of Martens's array scan latch organization 96 (*id.* at col. 5, ll. 25-27) that satisfies a need "to have the capability to read data out of the array serially in certain chip-testing conditions." *Id.* at col. 5, ll. 13-15.

Each of blocks 98, 100, and 106 (labeled "All Sense and Combination Circuitry for one array col.") is coupled to a respective column of the memory array. *Id.* at col. 5, ll. 25-40. In view of Figure 3, which shows the details of a sensing and combination circuit, it is apparent that each column constitutes a bitline (more particularly a group of bitline sections). As a

result, the data on array data outputs 116, 118, and 120 of blocks 98, 100, and 106 constitute n bits of a word that has been read out of memory.

As shown in Figure 4, the n bits of output data are applied to scannable latches 104, 102, and 108, respectively, which are connected in a way that permits the bit values of an output test word to be serially (i.e., sequentially) compared to an "expectation value":

> In addition to reading data out of the array during normal operation of the microprocessor, it is necessary to have the capability to read data out of the array serially in certain chip-testing conditions. This capability is referred to as scannability of the array. The capability of scannability (also referred to as "scan testing") requires that the array be able to hold its results in a group of memory elements. These memory elements are connected in series such that the output from the first memory element is fed to the scan input of the second element. The output of the last memory element is fed to a test circuit outside the array for comparison to some expectation value.

Id. at col. 5, ll. 13-24. Specifically, the scannability is provided by connecting scan output 130 of latch 104 to an input of latch 102, and by connecting scan output 132 of latch 102 to an input of latch 108, the scan output of which is connected to the input of the test circuit (not shown). *Id.* at col. 5, ll. 41-55.

Appellants' argument that "[t]here is no teaching that the output of the last memory element 108 includes sequentially extracted test words or that the test circuit (not shown in FIG. 4 of Martens) sequentially compares test bits with respective expected data bits" (Reply Br. 4) is unpersuasive. Although Martens does not describe the test words that are read out of memory and stored in the latches for later comparison with the "expectation value" as having "test bits" that are sequentially compared with "respective

test data bits" (the terms employed in the claim), Martens' test circuitry clearly operates in that manner. Because the latches can collectively store the bits of only one word at a time, the memory data must be extracted from the memory one word at a time (i.e., sequentially) for storage in the latches, as required by claim 11. Furthermore, the Examiner correctly found that "the comparison [in Martens] must be sequential, even though not explicitly stated, because the data being sequentially shifted out of SO output can only be compared serially/sequentially." Answer 12.

As for the additional requirement of claim 11 that the comparison occur "before extracting the next test word," Appellants have not separately argued that language, instead merely quoting it at pages 7 and 11 of the Brief and pages 2 and 4 of the Reply Brief together with the claim language that is specifically argued. For example, Appellants argue that the Examiner's hypothetical combination of Martens and Kim, even if obvious,

> is not enough to meet the claimed features of the invention, which requires sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits of the extracted test words with expected data bits with expected data bits, before extracting the next test word.

Reply Br. 4.

The only language of claim 11 that has not been addressed above is the requirement that the "memory array" (recited in the body of the claim) be a "sequential access memory array," as specified in the preamble, which reads, "A method of testing a sequential access memory array, the method comprising: . . . ." Martens's SRAM is not described as a sequential access memory array, such as a FIFO memory. For a teaching of a FIFO memory, the Examiner relies on Kim.

WHETHER IT WOULD HAVE BEEN OBVIOUS IN VIEW OF KIM TO APPLY MARTENS'S SCANNABILITY TEACHINGS TO A SEQUENTIAL MEMORY

For the following reasons, Appellants have not demonstrated that the Examiner erred in concluding that the subject matter of claim 11 would have been obvious in view of the combined teachings of Kim and Martens.

Kim discloses a technique for testing first-in-first-out (FIFO) memories in order to detect structural and functional faults. Kim, col. 1, ll. 5-7.

Kim's Figure 2 is reproduced below.

FIG. 2

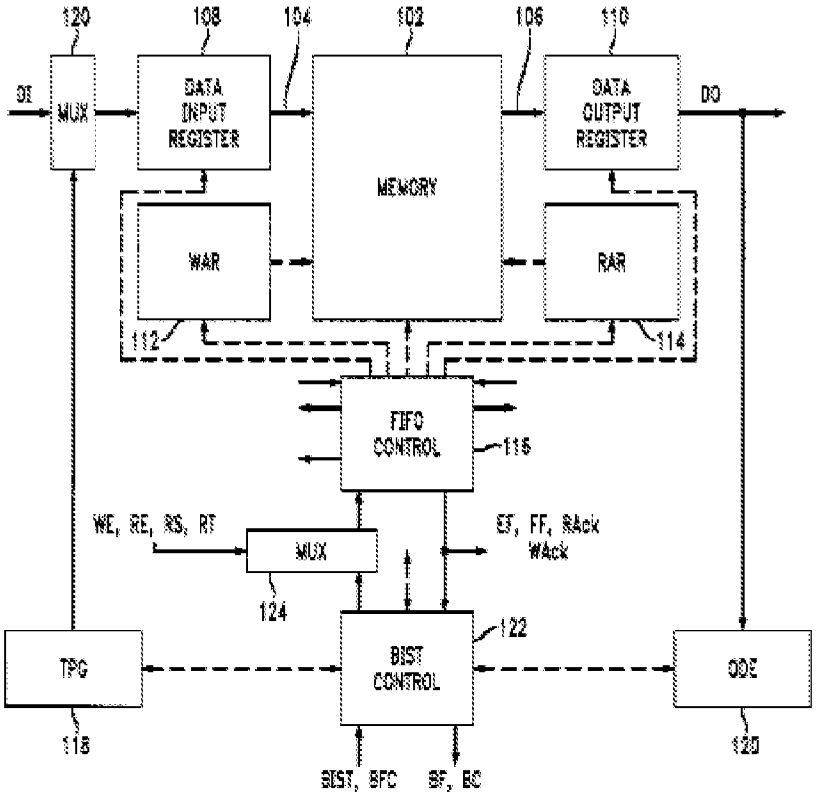

Figure 2 is a block schematic diagram of a FIFO having a dual-port RAM as its memory element and having Built-In Self-Test (BIST) features

to which Kim's invention may be applied. *Id.* at col. 4, ll. 24-27. Memory 102 is a random access memory having n storage rows or words and having separate input and output ports 104 and 106, respectively. *Id.* at col. 4, ll. 34-38. In Figure 1, memory 102 is specifically identified as an SRAM.

The BIST capability is provided by a BIST control 122, which controls a Test Pattern Generator (TPG) 118 and a Output Data Evaluator (ODE) 120. *Id.* at col. 6, ll. 23-25. The ODE 120, which is coupled to the output of the data output register (DOR) 110 so as to receive the same data that is output to the Data Output (DO) line, acts to compact or otherwise optimize the data output from the DO line during test intervals based on responses generated by the RAM 102 to the test patterns provided by the TPG 118. *Id.* at col. 6, ll. 37-42.

Figure 3 is reproduced below.

FIG. 3

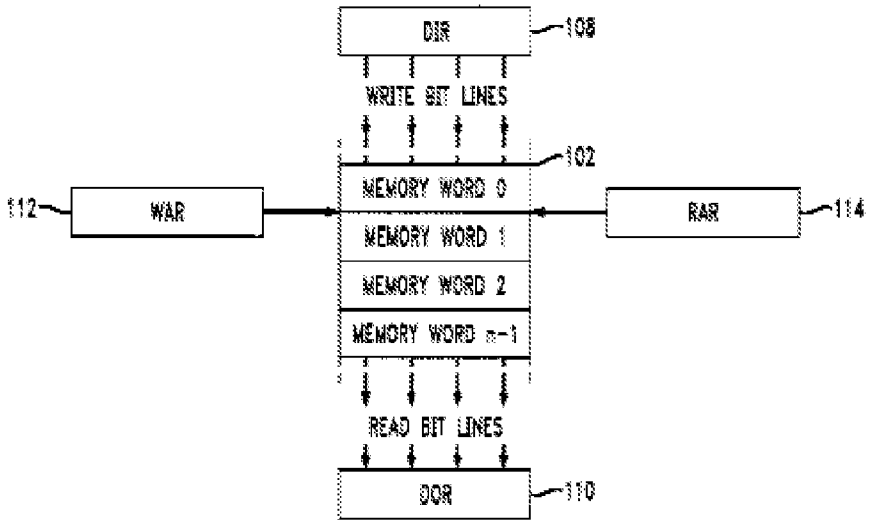

Figure 3 is a block schematic diagram of a portion of the FIFO of Figure 1 showing the manner in which the RAM is addressed. *Id.* at col. 4,

ll. 28-30. Figure 3 shows that words are sequentially extracted from the memory for storage in DOR 110.

As explained above, Martens's scannable latches, which are used with an SRAM, satisfy the above-noted need "to have the capability to read data out of the array serially in certain chip-testing conditions" (Martens, col. 5, ll. 13-15), an objective that Martens achieves with minimum size and minimum delay. *See id.* at col. 8, ll. 50-53 ("By utilizing this [disclosed] circuit, the best overall combination of key criteria is realized: minimum size, minimum delay, and proper testability (i.e., scannability)."). We find that a person having ordinary skill in the art would have recognized that the foregoing benefits would be applicable to an SRAM that is operated as a sequential access (i.e., FIFO) memory and therefore conclude that it would have been obvious in view of Kim to employ Martens's scannable latches with a sequential access memory, such as by operating Martens's SRAM memory as a sequential (i.e., FIFO) memory. *See KSR*, 550 U.S. at 417 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill."). Appellants have not asserted, let alone demonstrated, that the application of Martens's scannable latching technique to an SRAM that is being used as a sequential (i.e., FIFO) memory would have been beyond the skill of a person having ordinary skill in the relevant art.

Because the above combination of reference teachings does not rely on the type of memory testing that is performed by Kim's ODE (output data evaluator) 120, it is not necessary to address Appellants' argument that Kim

"fail[s] to teach sequentially extracting test words from the memory plane and sequentially comparing the test bits with the expected binary data bits, as claimed." Reply Br. 3.

CONCLUSIONS

Appellants have not shown that the Examiner erred in finding that Martens discloses (1) sequentially extracting the test words from the memory array and (2) sequentially comparing the test bits of the extracted test words with the expected data bits for each extracted test word. Nor have Appellants shown that the Examiner erred in concluding that it would have been obvious in view of Kim to apply Martens's teachings to a sequential access memory.

We therefore affirm the obviousness rejection of representative claim 11 as well as the obviousness rejections of claims 9, 12, 14-17, 20-23, and 26-29, which are not separately argued.

DECISION

The rejection of claims 9, 11, 14-17, 20-23, and 26-29 under 35 U.S.C. § 103(a) for obviousness over Kim in view of Martens is affirmed, as is the rejection of claim 12 under § 103(a) for obviousness over Kim in view of Martens and Zorian.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. §§ 41.50(f) and 41.52(b).

AFFIRMED

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